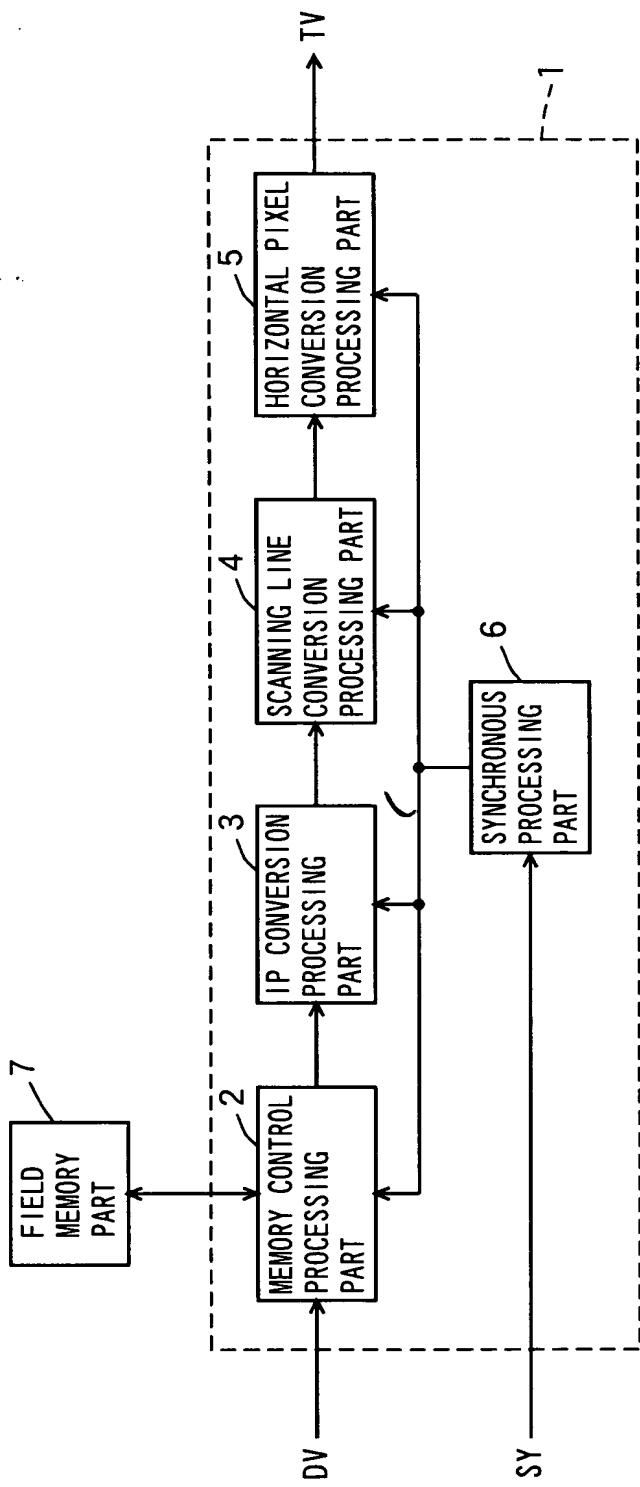


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FIG. 1



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FIG. 2

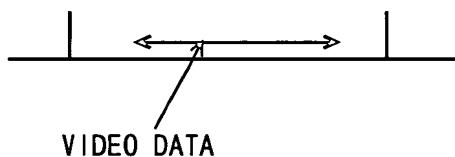
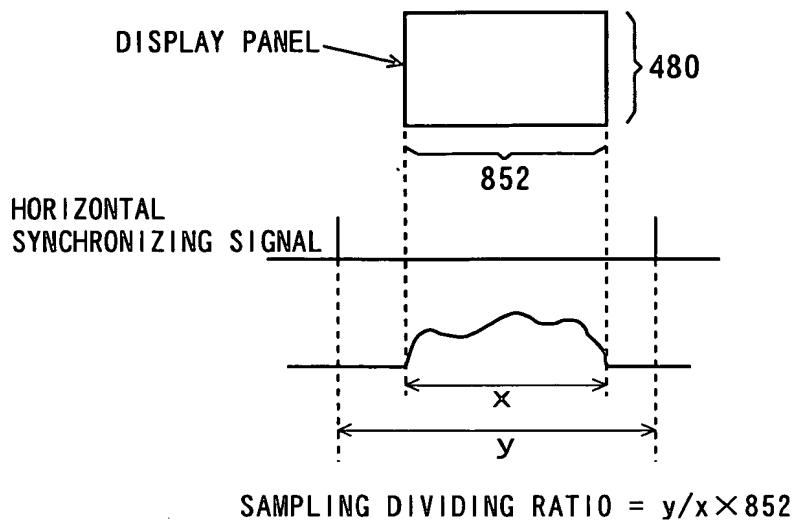
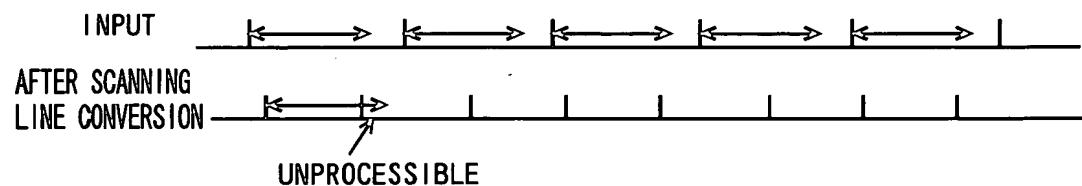


FIG. 3

(a) CASE OF CLOCK IDENTICAL TO INPUT



(b) CASE OF CLOCK SUFFICIENTLY QUICK AS COMPARED WITH INPUT

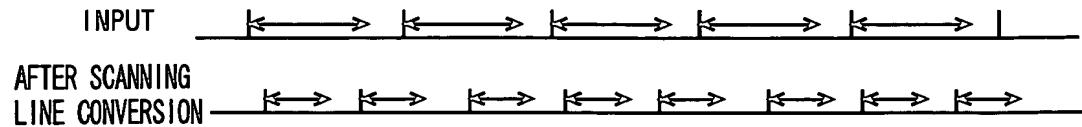
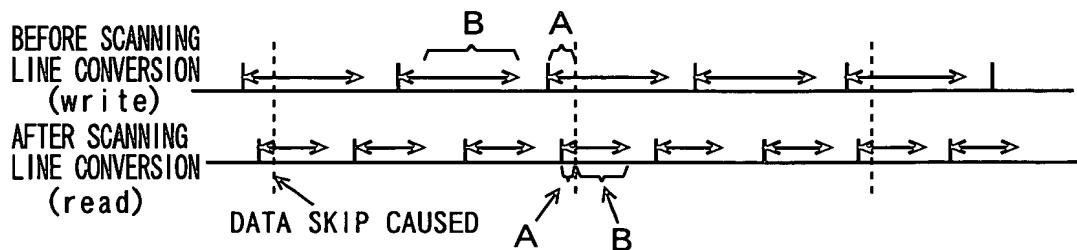
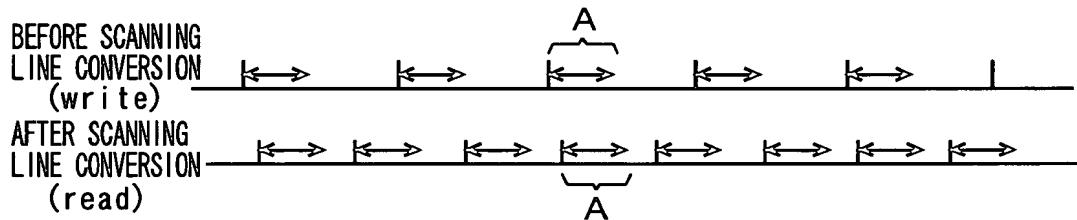


FIG. 4

(a) WHEN TRANSFERRING CLOCK BEFORE AND AFTER SCANNING LINE CONVERSION

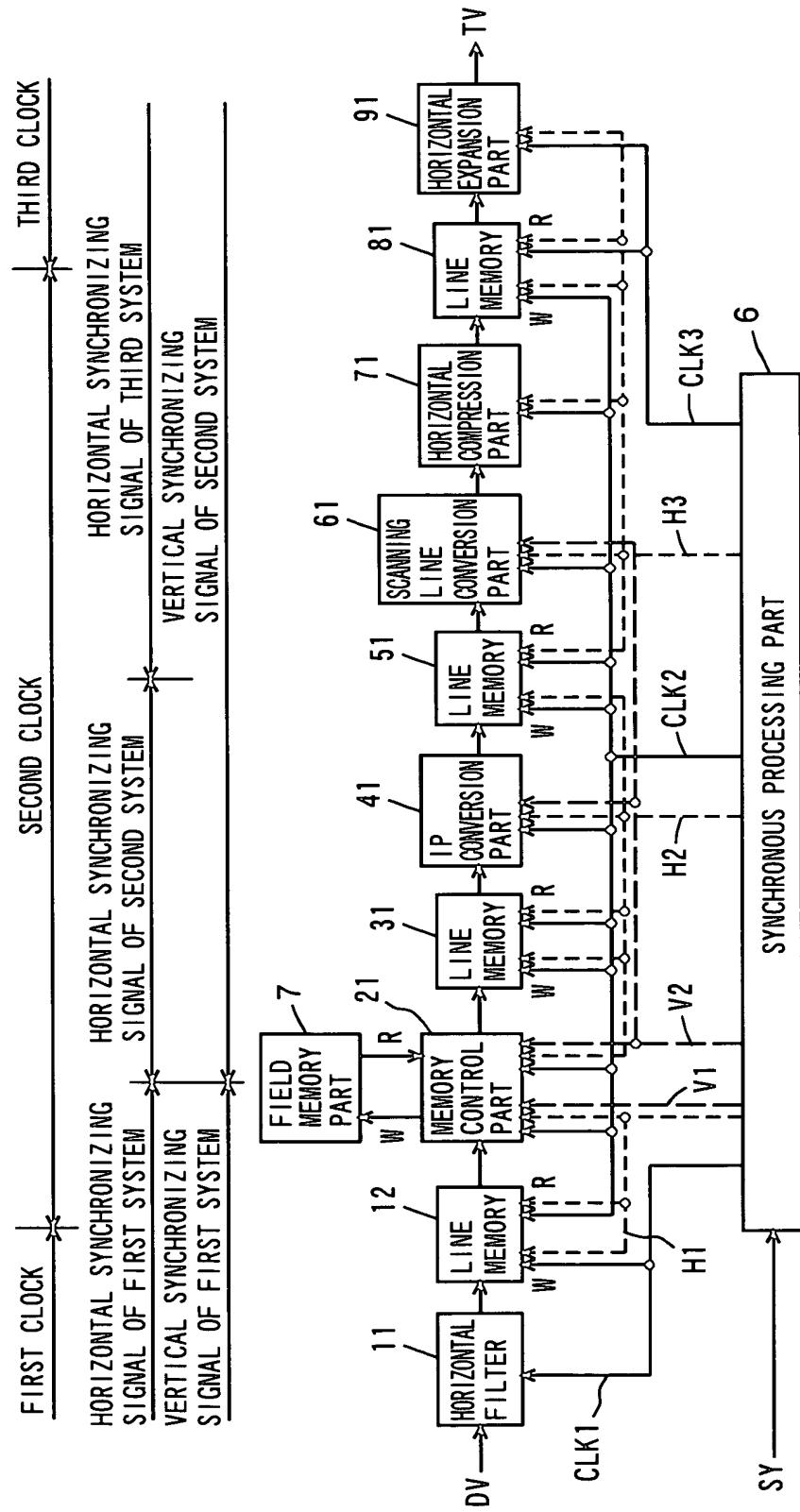


(b) WHEN TRANSFERRING CLOCK AFTER SCANNING LINE CONVERSION



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FIG. 5



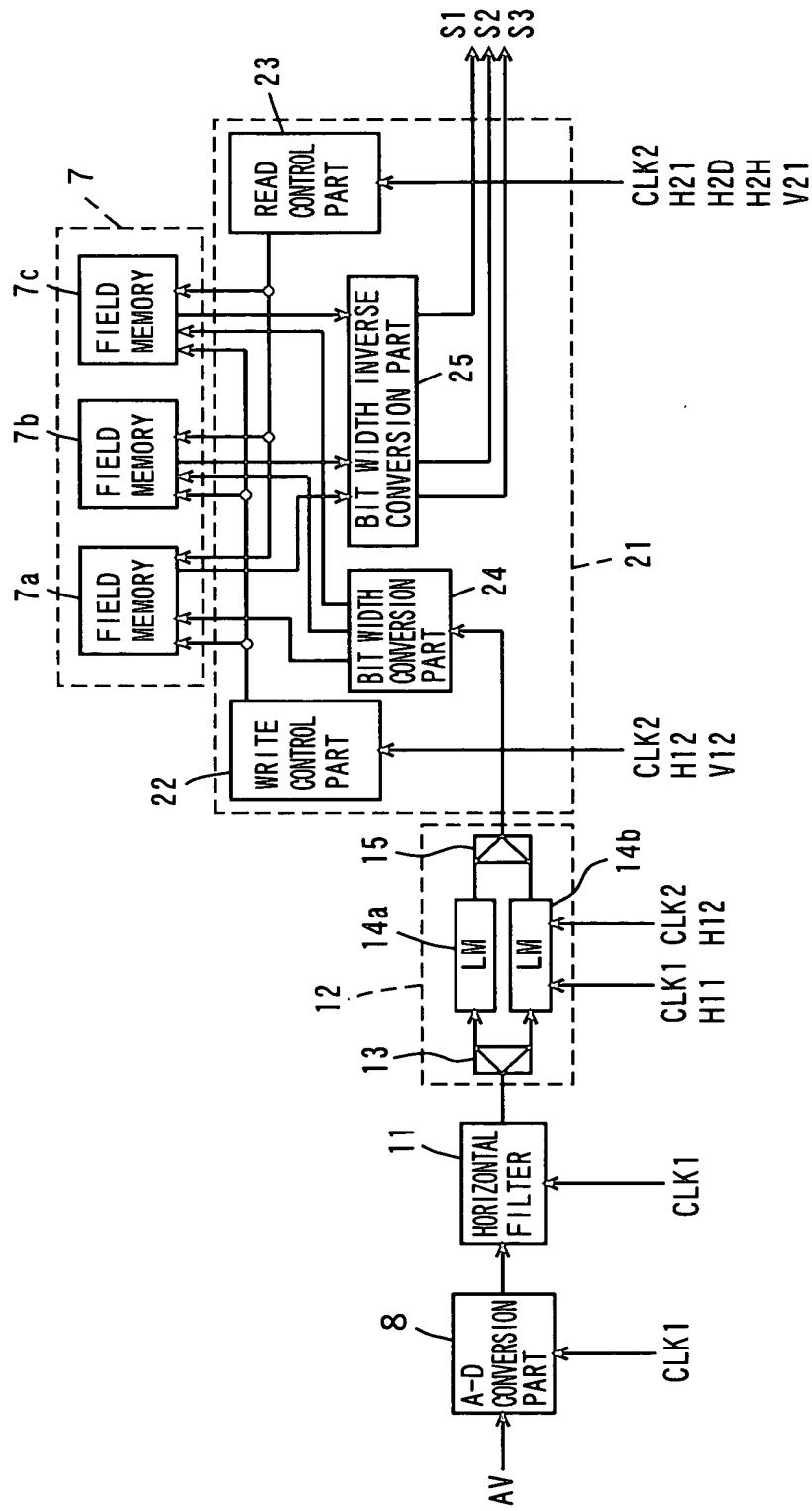
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FIG. 6

		WITH IP CONVERSION		WITH NO IP CONVERSION	
		ODD FIELD	EVEN FIELD		
CLK1 SYSTEM					
H11(INPUT H)					
V11(INPUT V)					
CLK2 SYSTEM					
H12(LATCH CLK2 OF H11)					
V12(LATCH CLK2 OF V11)					
H21(H AFTER FIELD MEMORY)					
H2D(DELAYED BY HALF H OF H21)					
H2H(DOUBLE FREQUENCY OF H21)					
V21(V AFTER FIELD MEMORY)					
H31(H AFTER SCANNING LINE CONVERSION)					
V2P(V AFTER SCANNING LINE CONVERSION)					
CLK3 SYSTEM					
H33(LATCH CLK3 OF H31)					

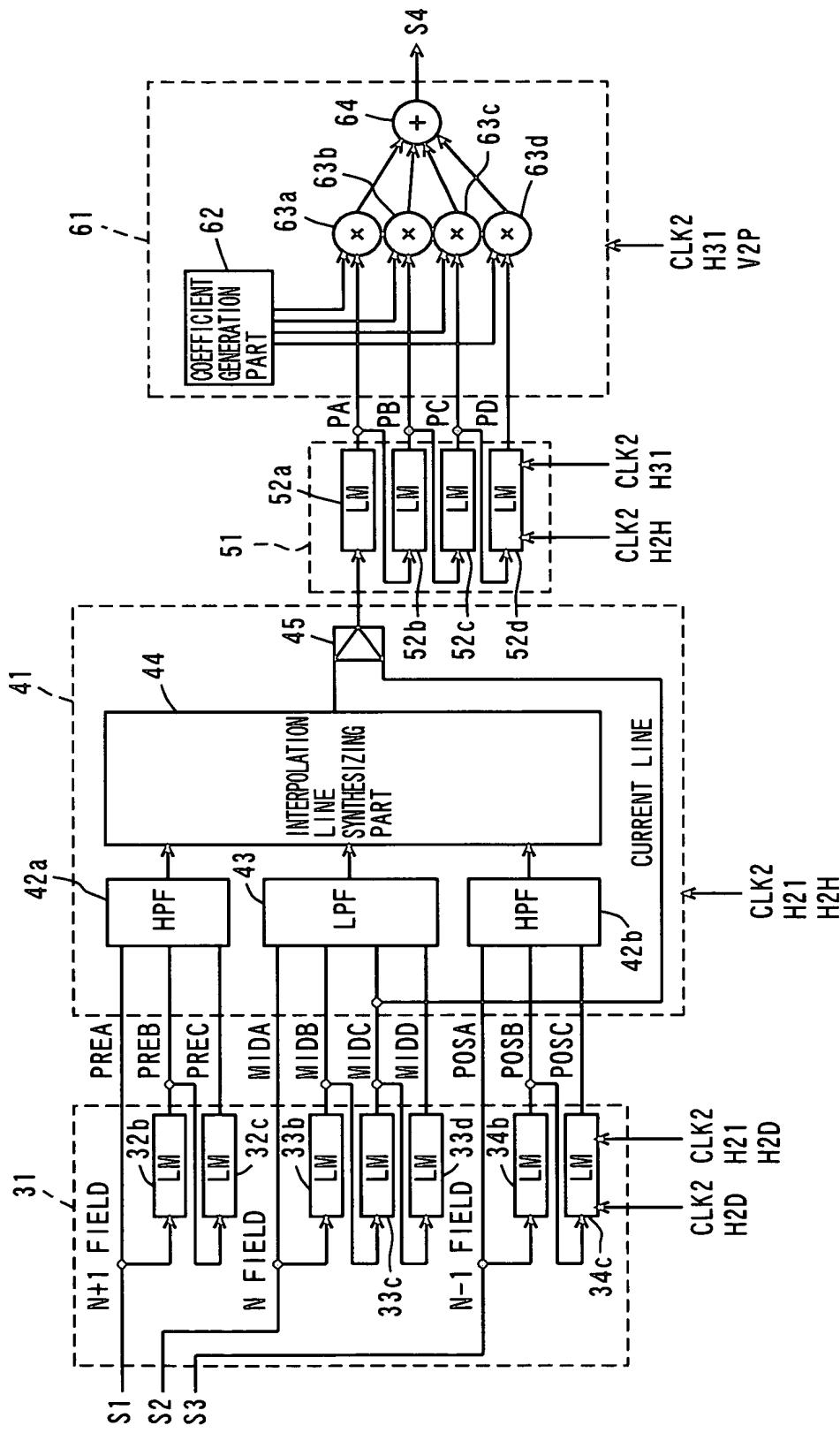
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FIG. 7



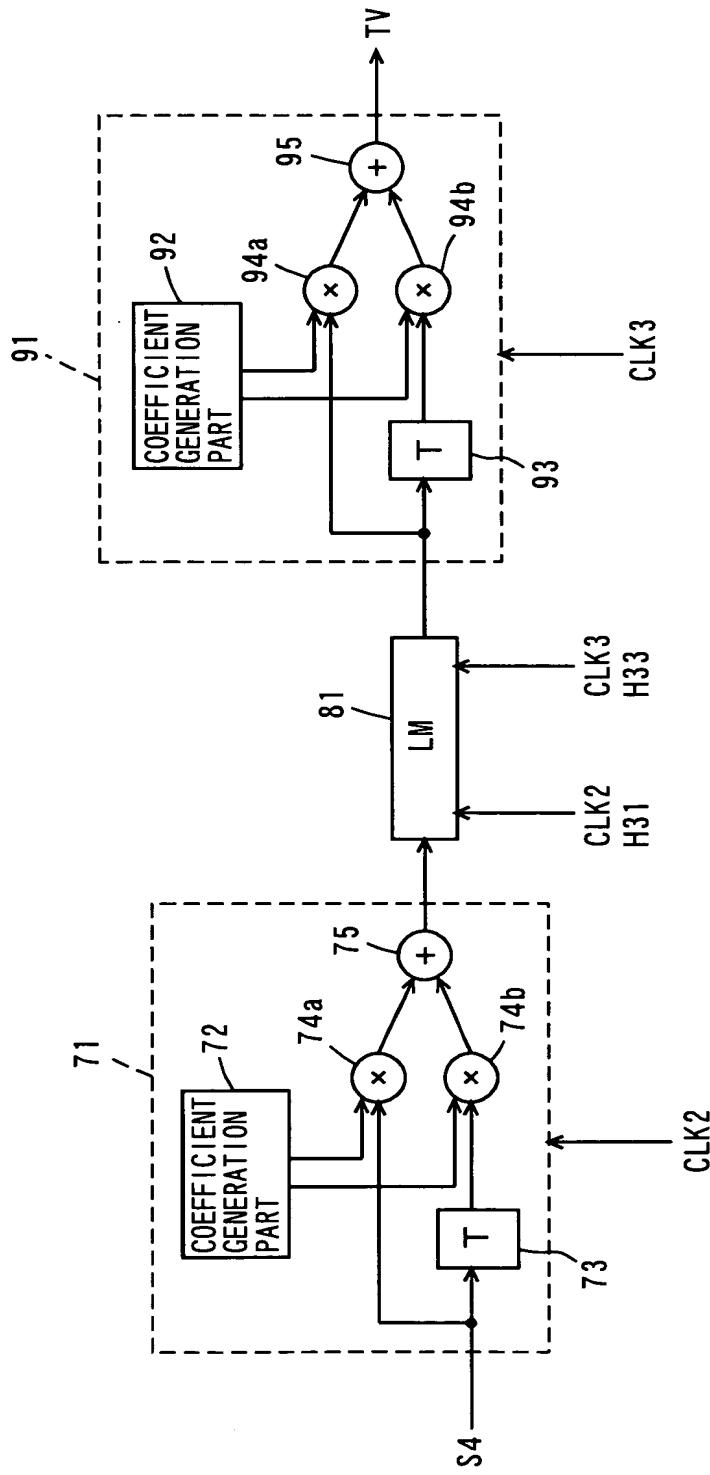
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FIG. 8



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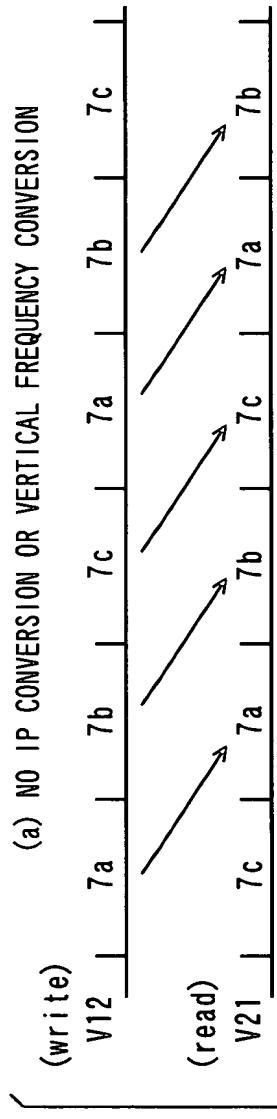
FIG. 9



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FIG. 10

(a) NO IP CONVERSION OR VERTICAL FREQUENCY CONVERSION



(b) IP CONVERSION

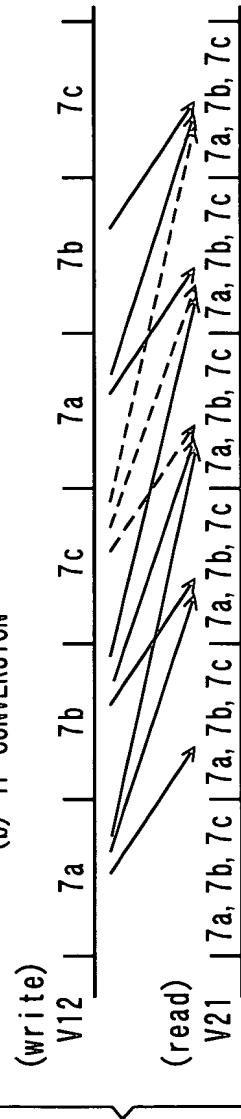
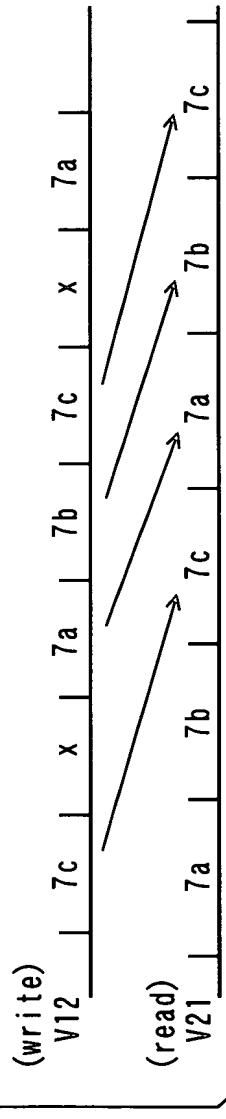
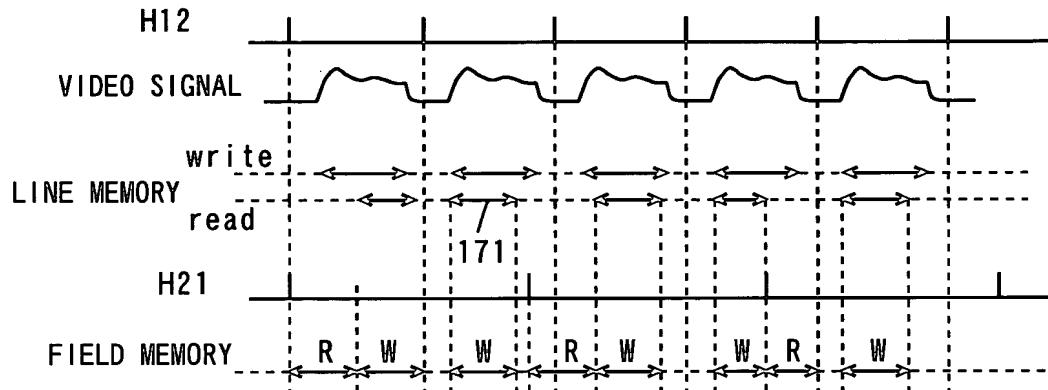
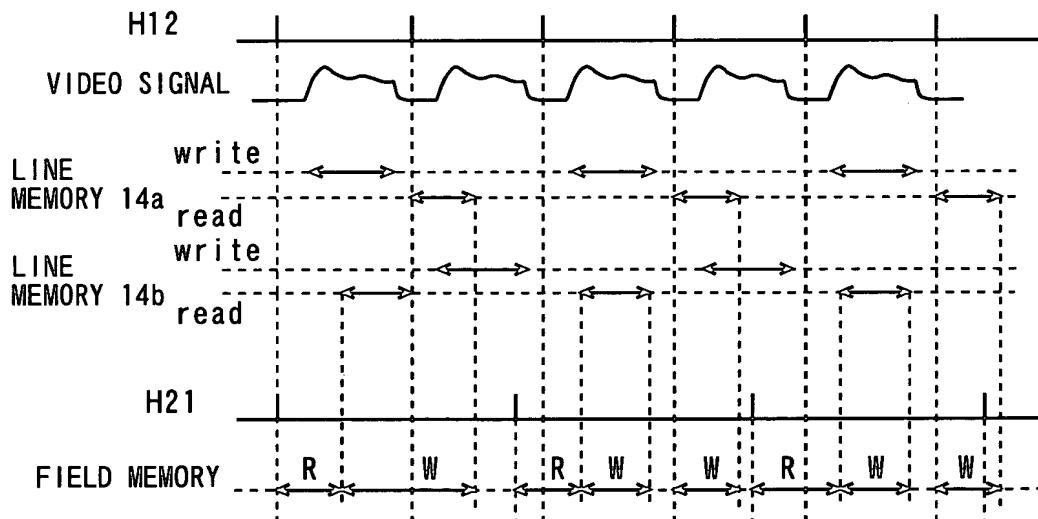
(c) VERTICAL FREQUENCY CONVERSION
EXAMPLE: 4 → 3 CONVERSION

FIG. 11

(a) WITH ONE LINE MEMORY

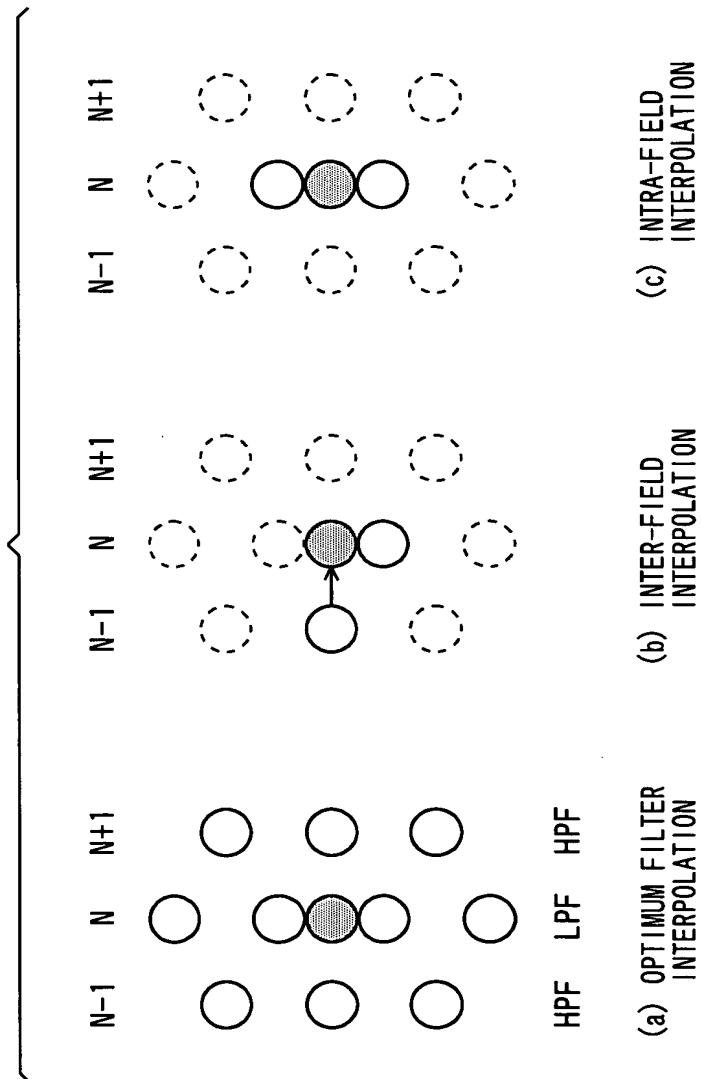


(b) WITH TWO LINE MEMORIES



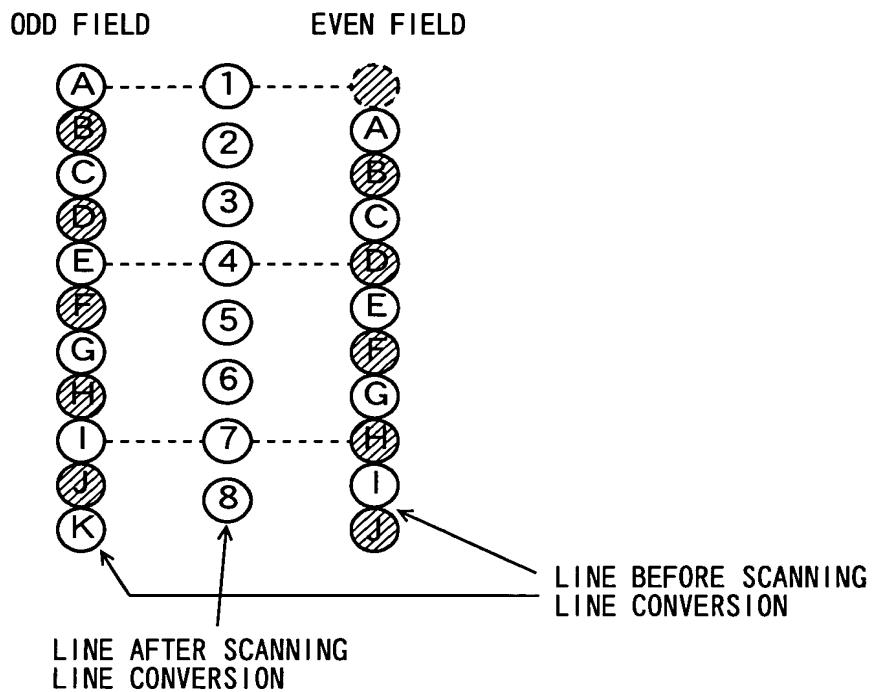
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FIG. 12



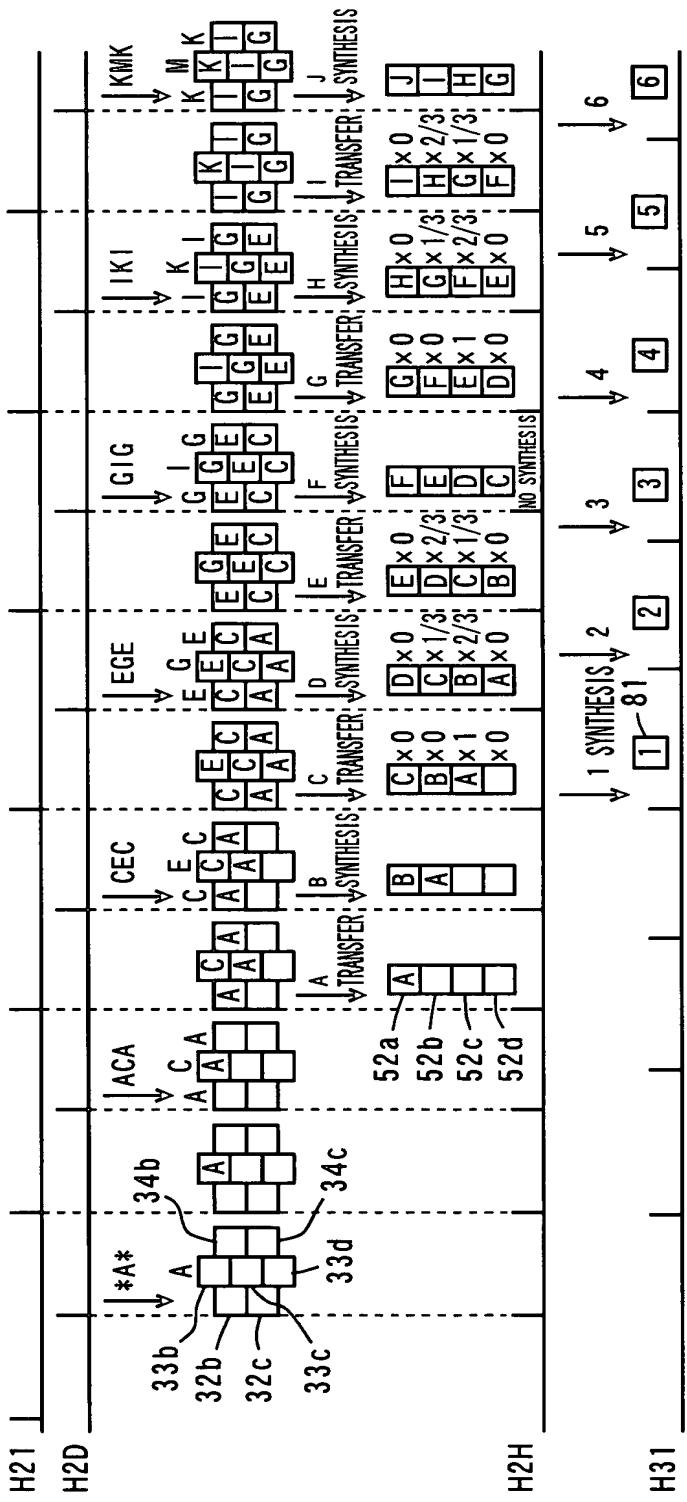
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FIG. 13



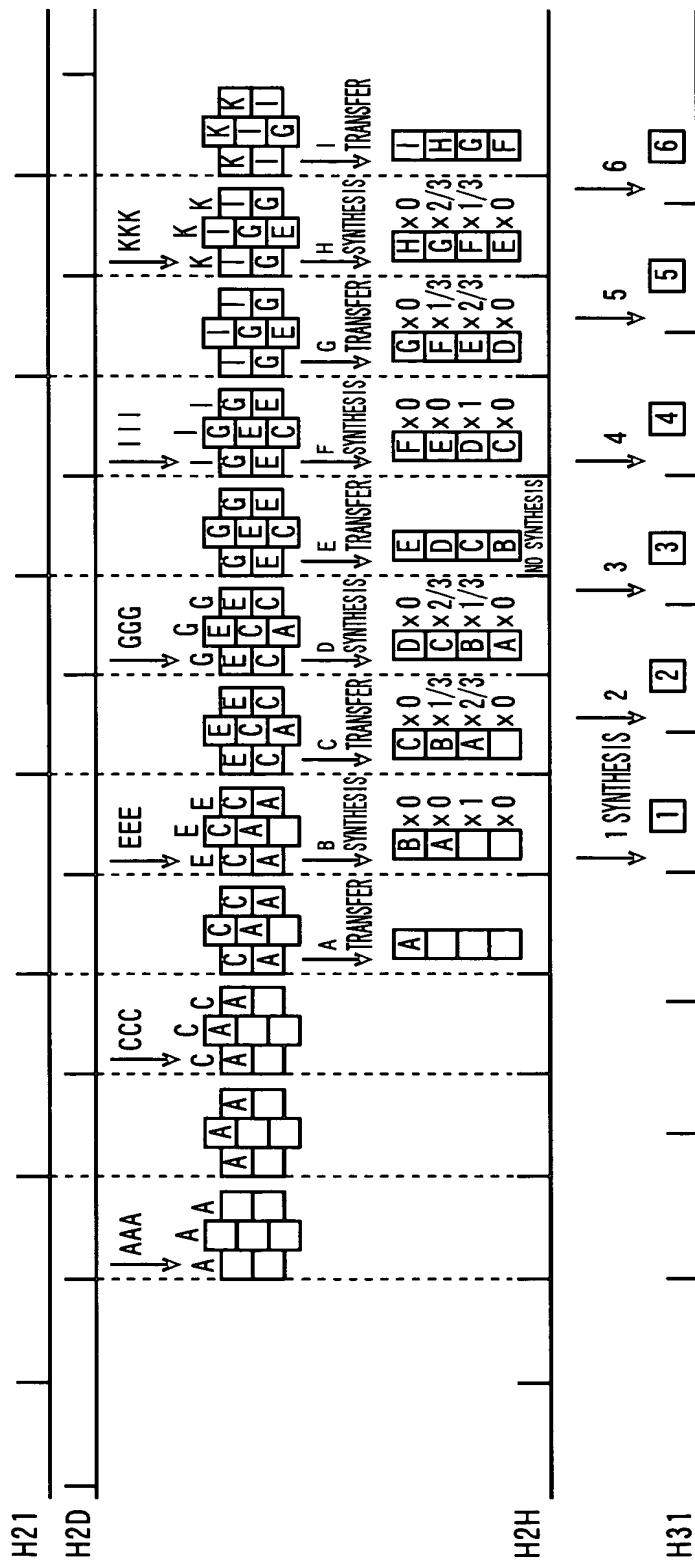
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F - G. 1 4



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F - G. 1 5



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FIG. 16

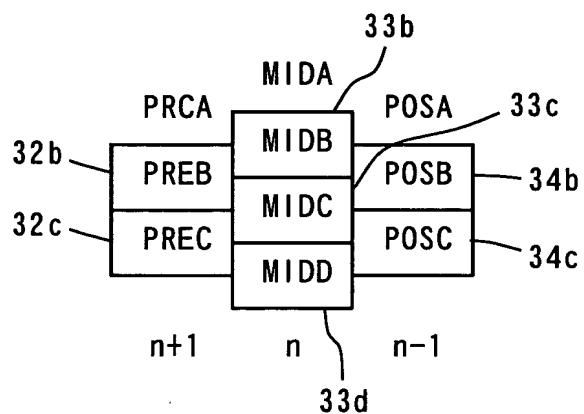
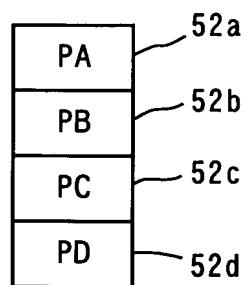
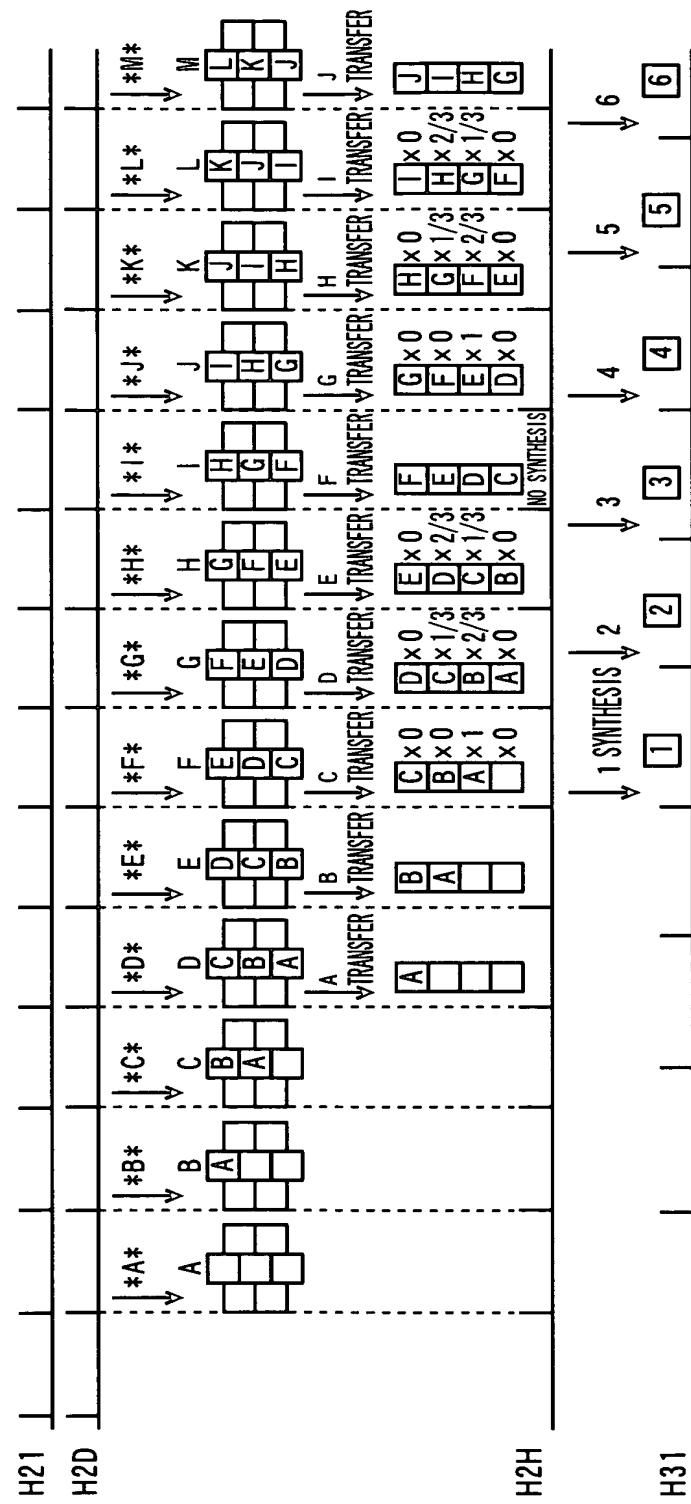


FIG. 17



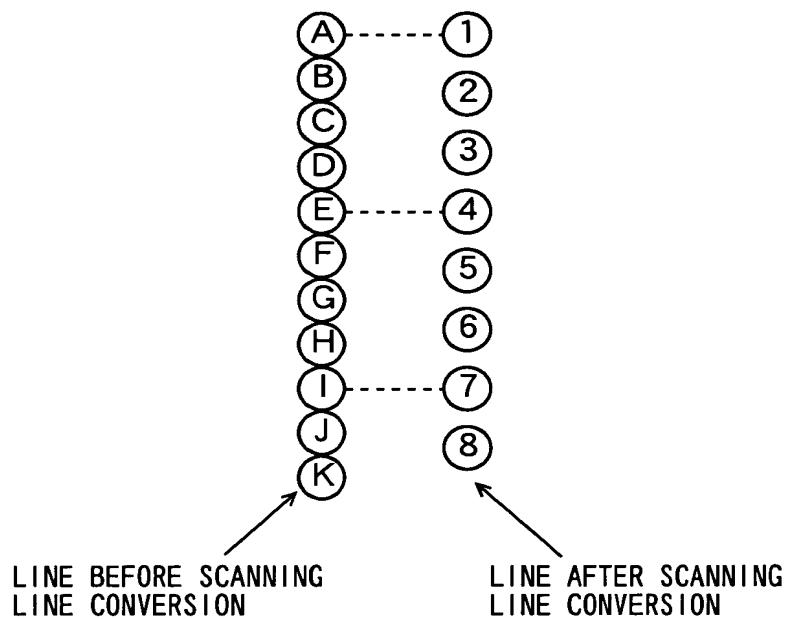
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FIG. 18



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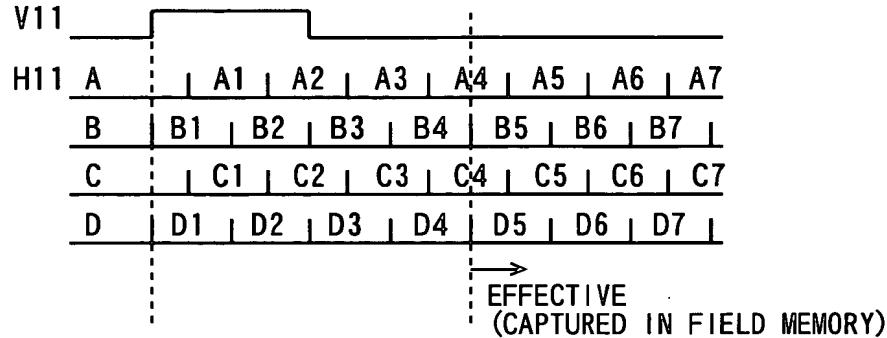
FIG. 19



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FIG. 20

(a) INPUT



(b) OUTPUT SEQUENCE FROM FIELD MEMORY (ODD FIELD)

V21

H21

H2D

START FIELD MEMORY TRANSFER

	*	*	*	B5	-	B6	-	B7	-	B8	-	B9	-	B10	-		
MIDA	*	*	*	*	*	B5	-	B6	-	B7	-	B8	-	B9	-		
MIDB	*	*	*	*	*	*	B5	-	B6	-	B7	-	B8	-	B9	-	
MIDC	*	*	*	*	*	*	B5	B5	B6	B6	B7	B7	B8	B8	B9	-	
MIDD	*	*	*	*	*	*	*	*	*	*	*	B5	-	B6	-	B7	-
POSA	*	*	*	*	*	A5	-	A6	-	A7	-	A8	-	A9	-		
POSB	*	*	*	*	*	*	A5	-	A6	-	A7	-	A8	-			
POSC	*	*	*	*	*	*	*	*	*	A5	-	A6	-	A7	-		
PREA	*	*	*	*	*	C5	-	C6	-	C7	-	C8	-	C9	-		
PREB	*	*	*	*	*	*	C5	-	C6	-	C7	-	C8	-			
PREC	*	*	*	*	*	*	*	*	*	C5	-	C6	-	C7	-		

(c) OUTPUT SEQUENCE FROM FIELD MEMORY (EVEN FIELD)

V21

H21

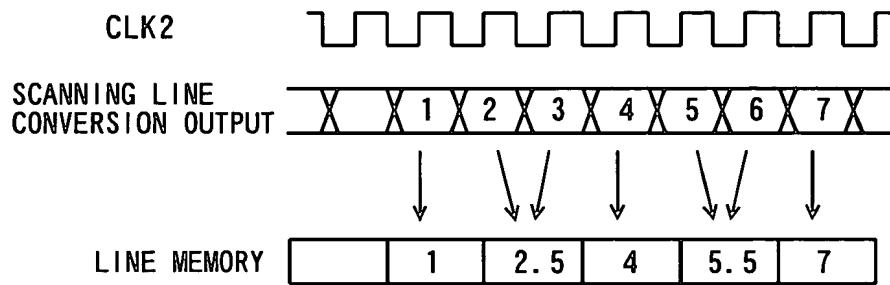
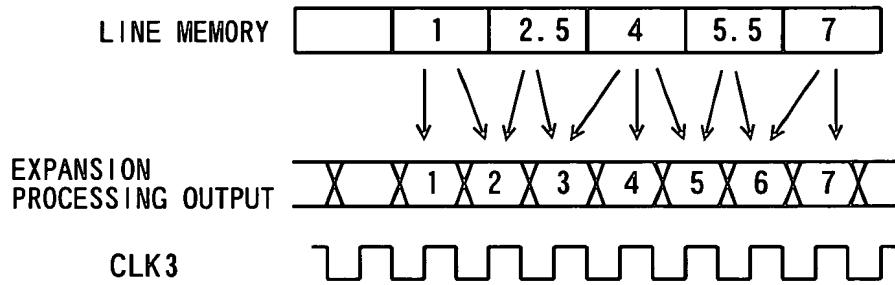
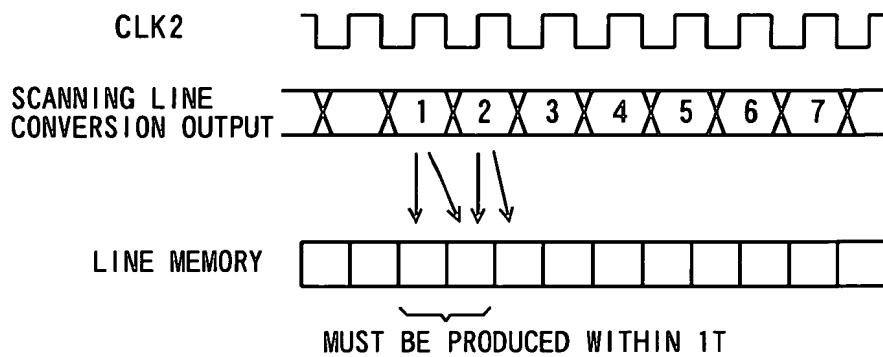
H2D

START FIELD MEMORY TRANSFER

	*	*	*	C5	-	C6	-	C7	-	C8	-	C9	-	C10	-		
MIDA	*	*	*	*	C5	-	C6	-	C7	-	C8	-	C9	-	C10	-	
MIDB	*	*	*	*	*	*	C5	-	C6	-	C7	-	C8	-	C9	-	
MIDC	*	*	*	*	*	*	*	C5	C5	C6	C6	C7	C7	C8	C8	-	
MIDD	*	*	*	*	*	*	*	*	*	*	*	C5	-	C6	-	C7	-
POSA	*	*	*	*	B5	-	B6	-	B7	-	B8	-	B9	-	B10	-	
POSB	*	*	*	*	*	*	B5	-	B6	-	B7	-	B8	-	B9	-	
POSC	*	*	*	*	*	*	*	*	B5	-	B6	-	B7	-	B8	-	
PREA	*	*	*	*	D5	-	D6	-	D7	-	D8	-	D9	-	D10	-	
PREB	*	*	*	*	*	*	D5	-	D6	-	D7	-	D8	-	D9	-	
PREC	*	*	*	*	*	*	*	*	D5	-	D6	-	D7	-	D8	-	

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FIG. 21

(a) WRITING ($3 \rightarrow 2$ CONVERSION)(b) READING ($2 \rightarrow 3$ CONVERSION)(c) WRITING COMBINED WITH EXPANSION PROCESSING ($3 \rightarrow 4$ CONVERSION)

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FIG. 22

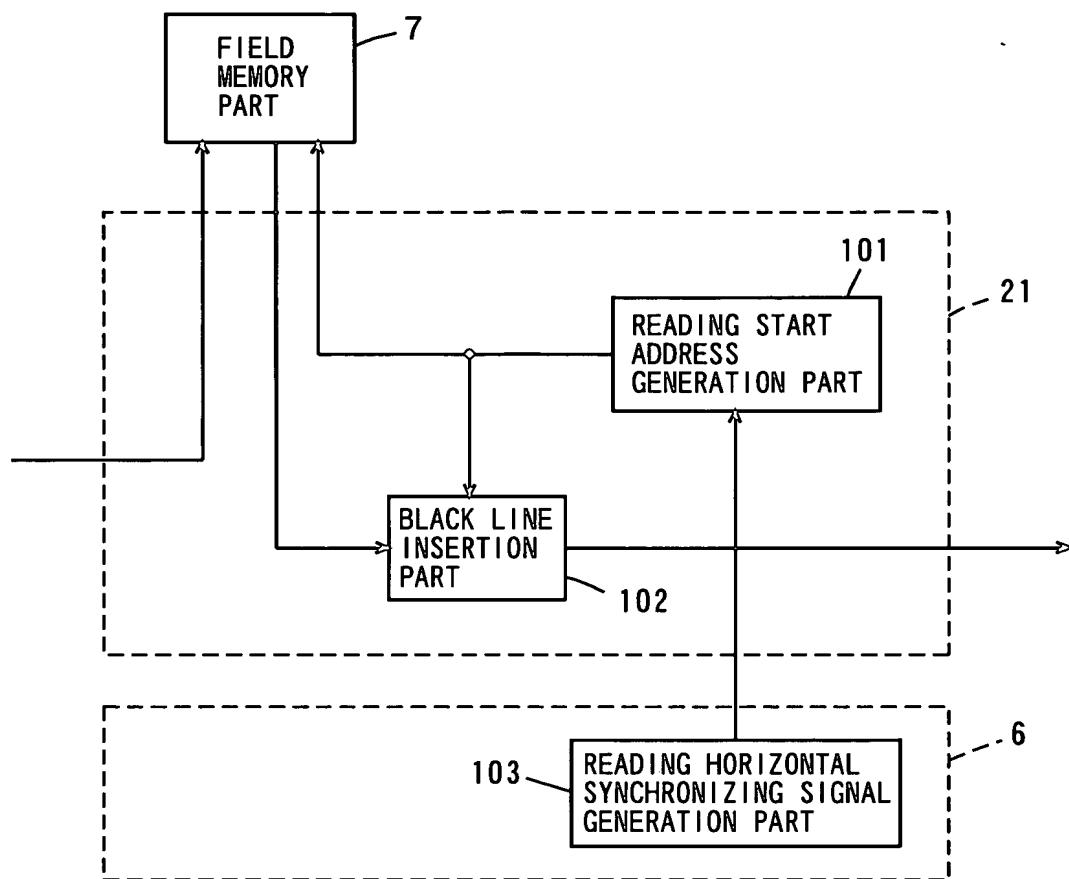
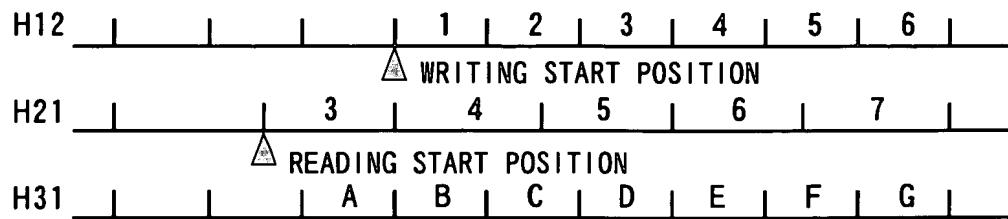


FIG. 23



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FIG. 24

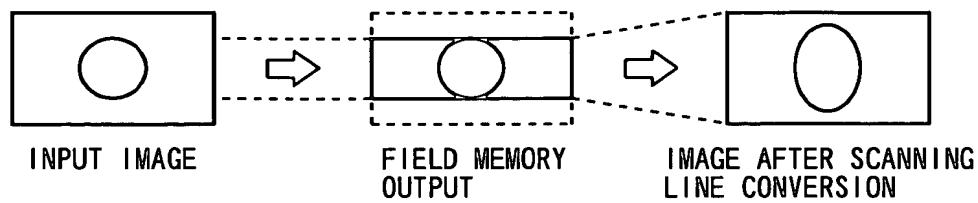


FIG. 25

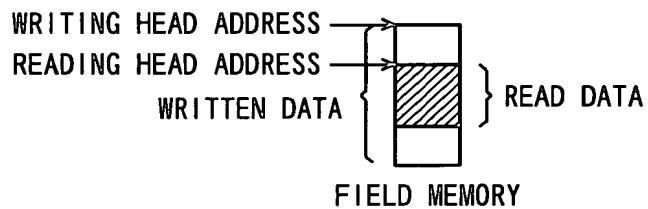
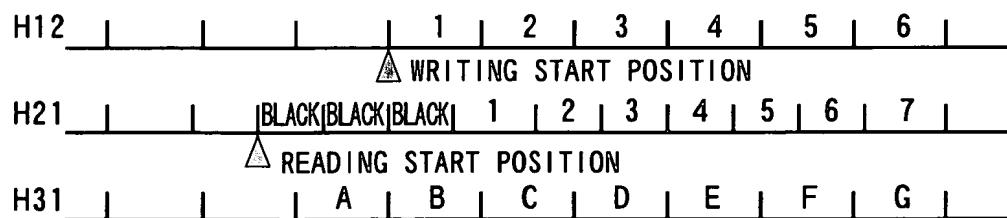


FIG. 26



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FIG. 27

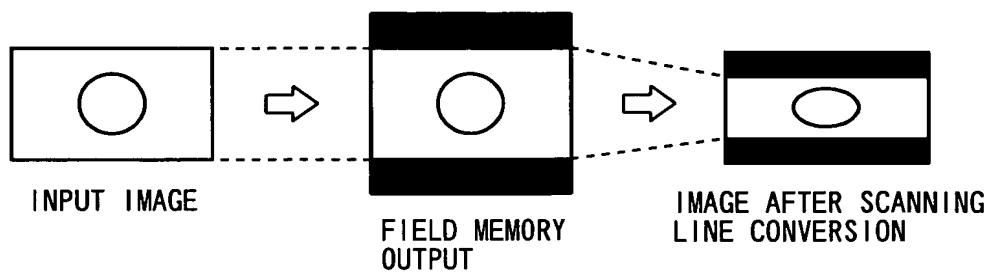
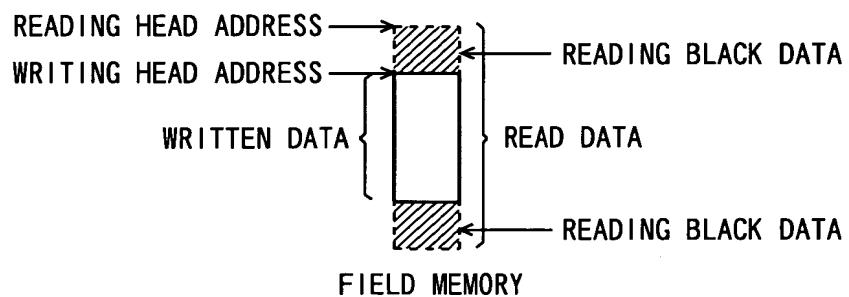
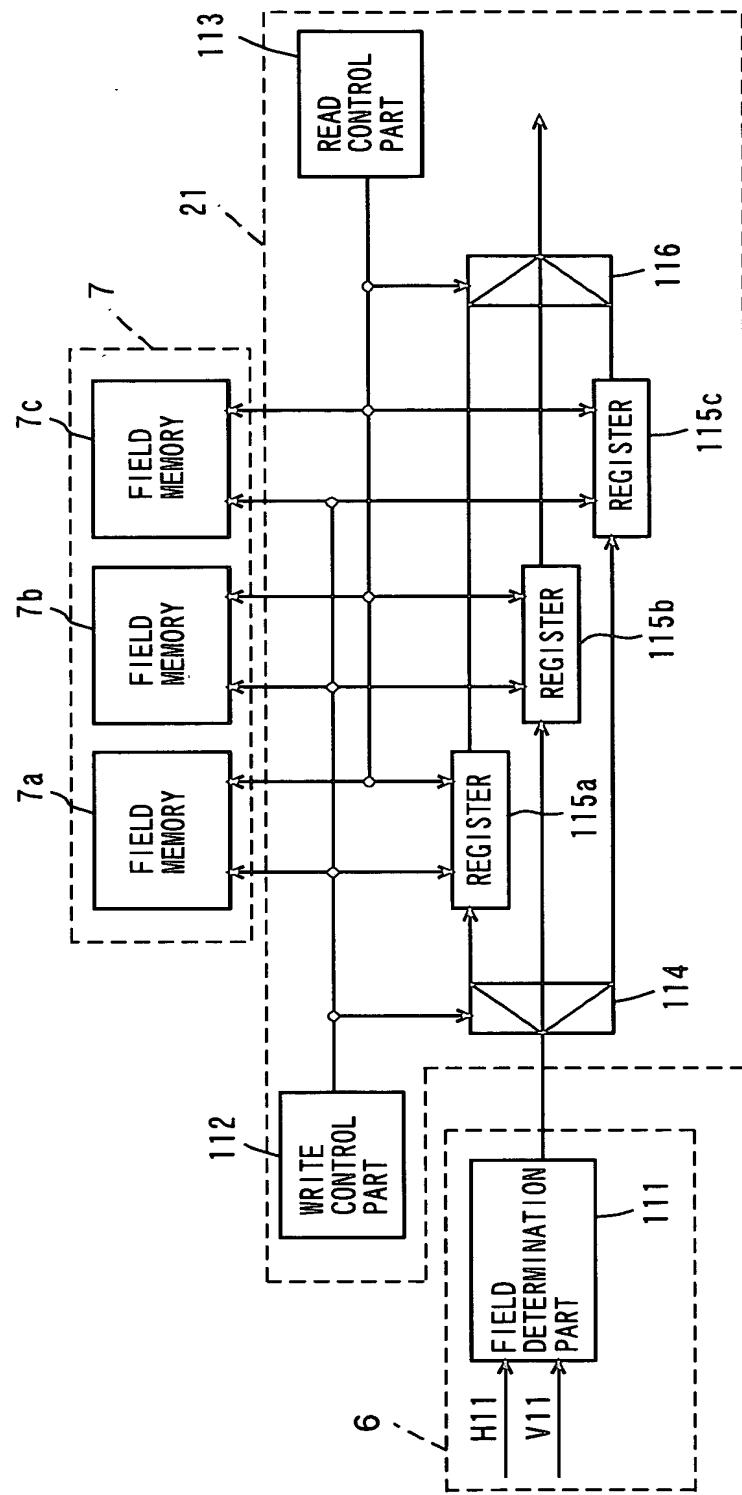


FIG. 28



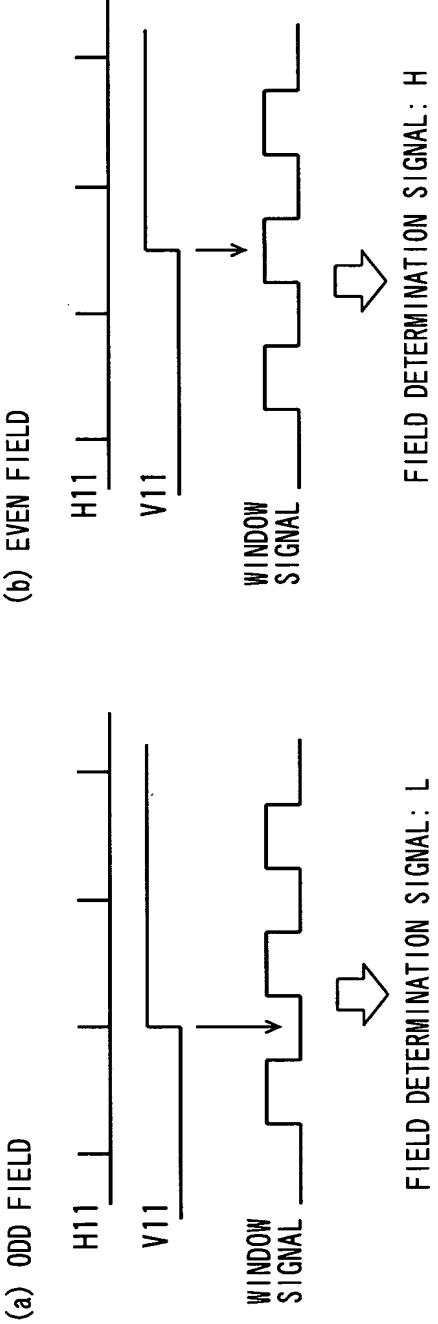
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FIG. 29



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FIG. 30

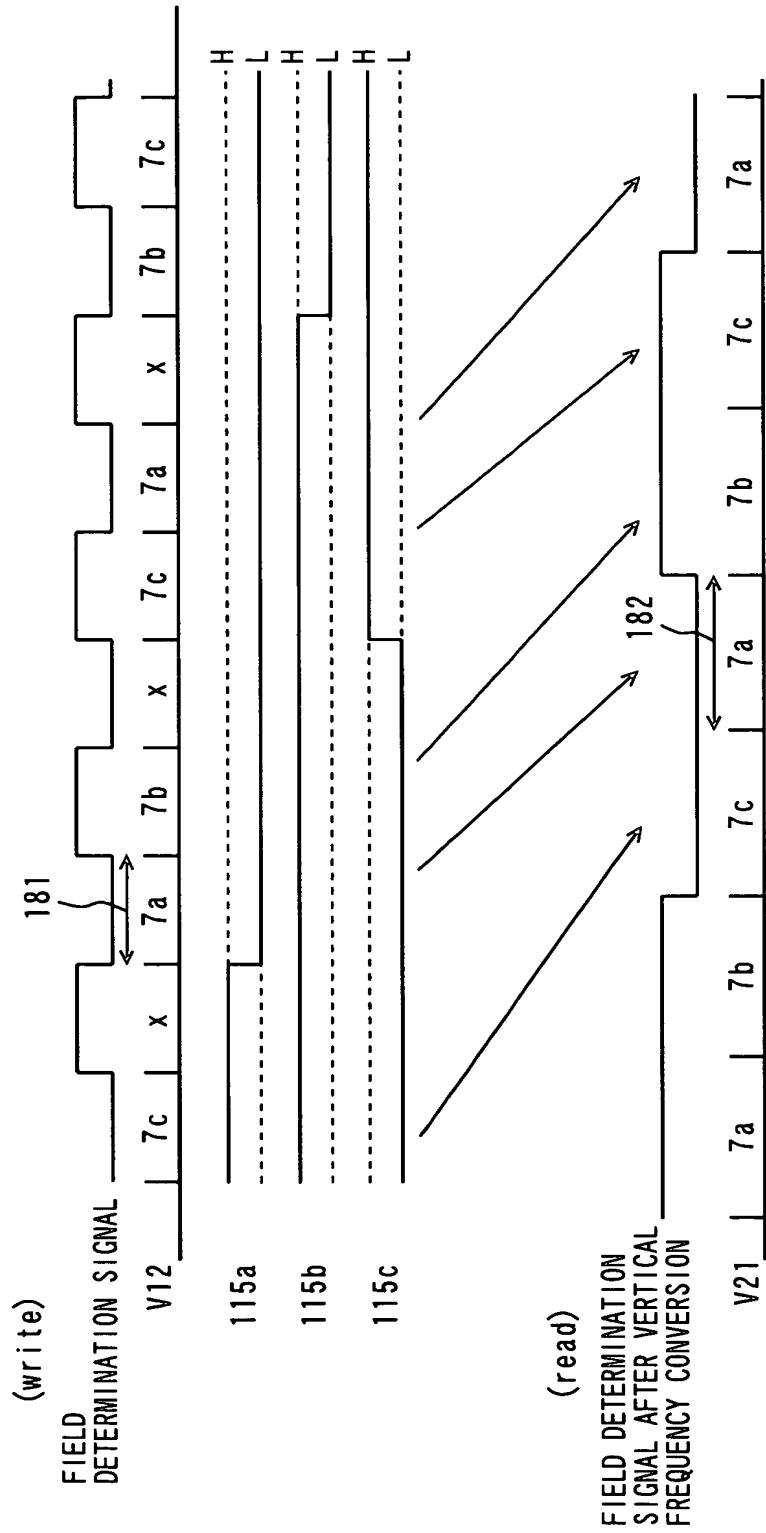


FIELD DETERMINATION SIGNAL: L

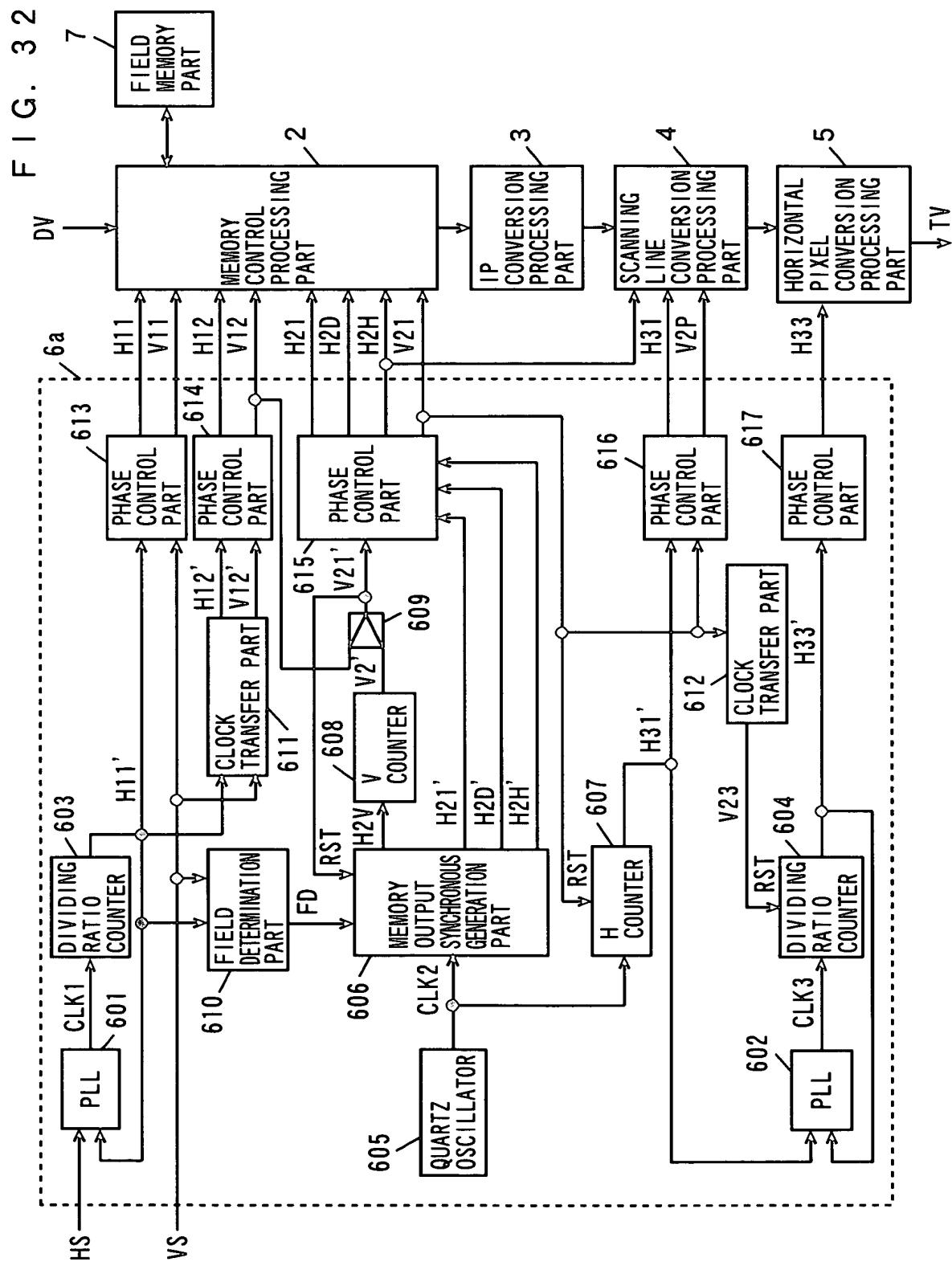
FIELD DETERMINATION SIGNAL: H

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FIG. 31



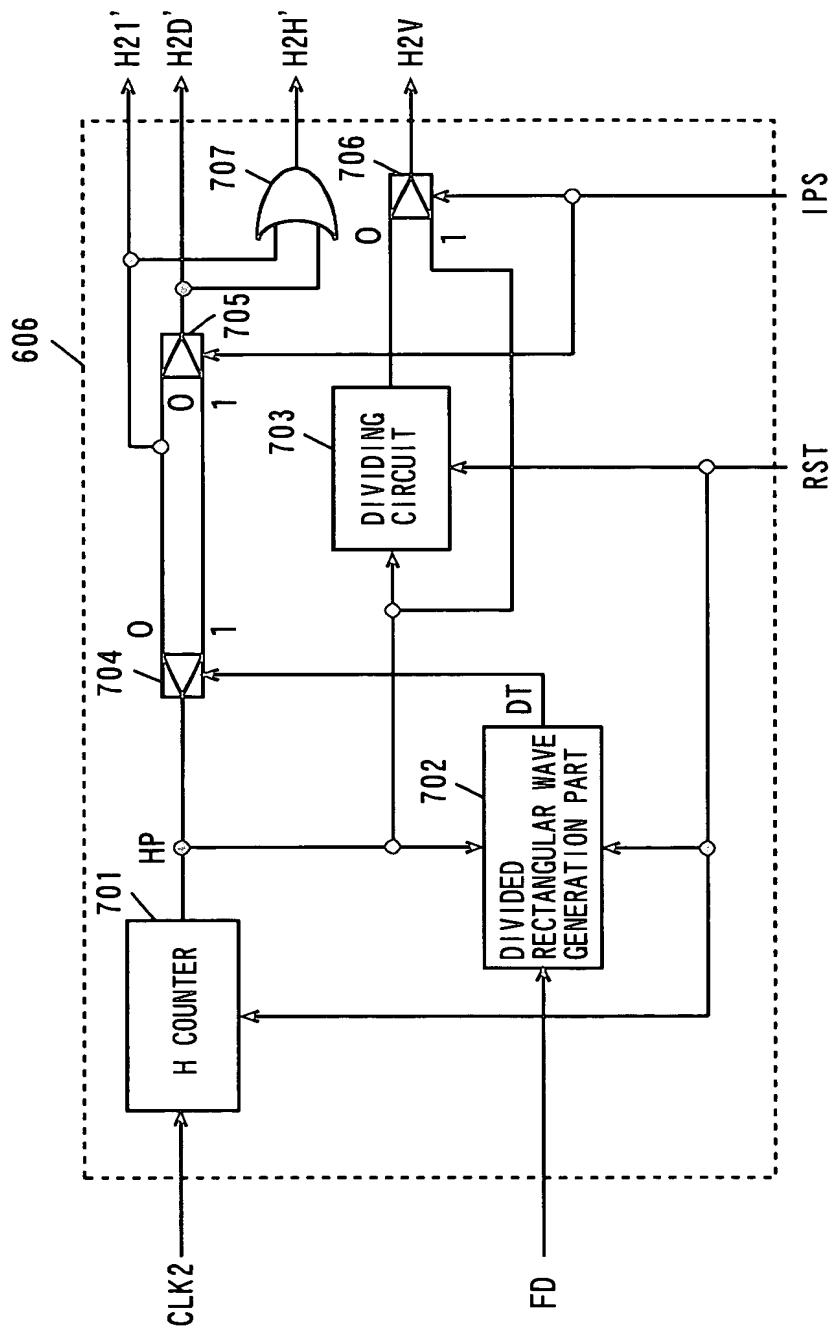
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FIG. 33



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F I G. 34

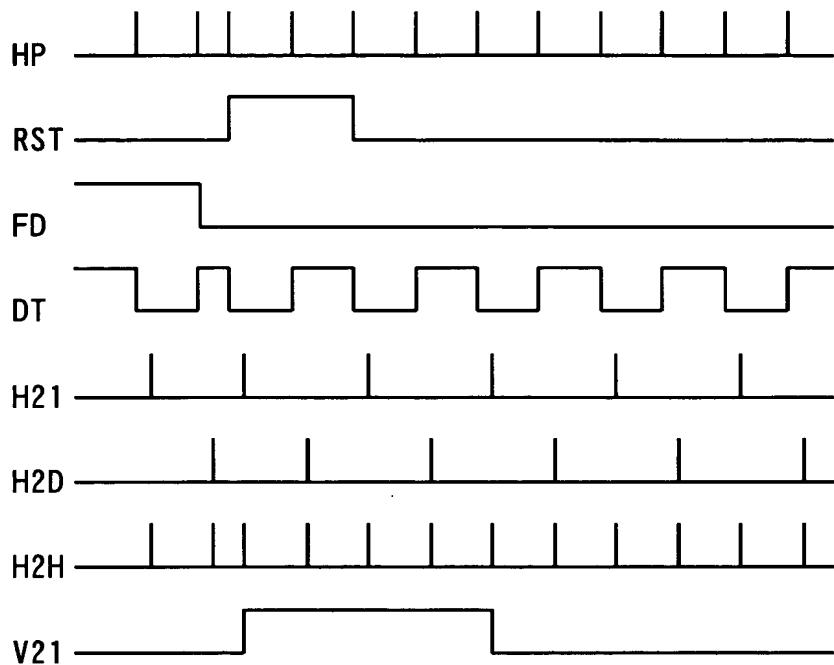


FIG. 35

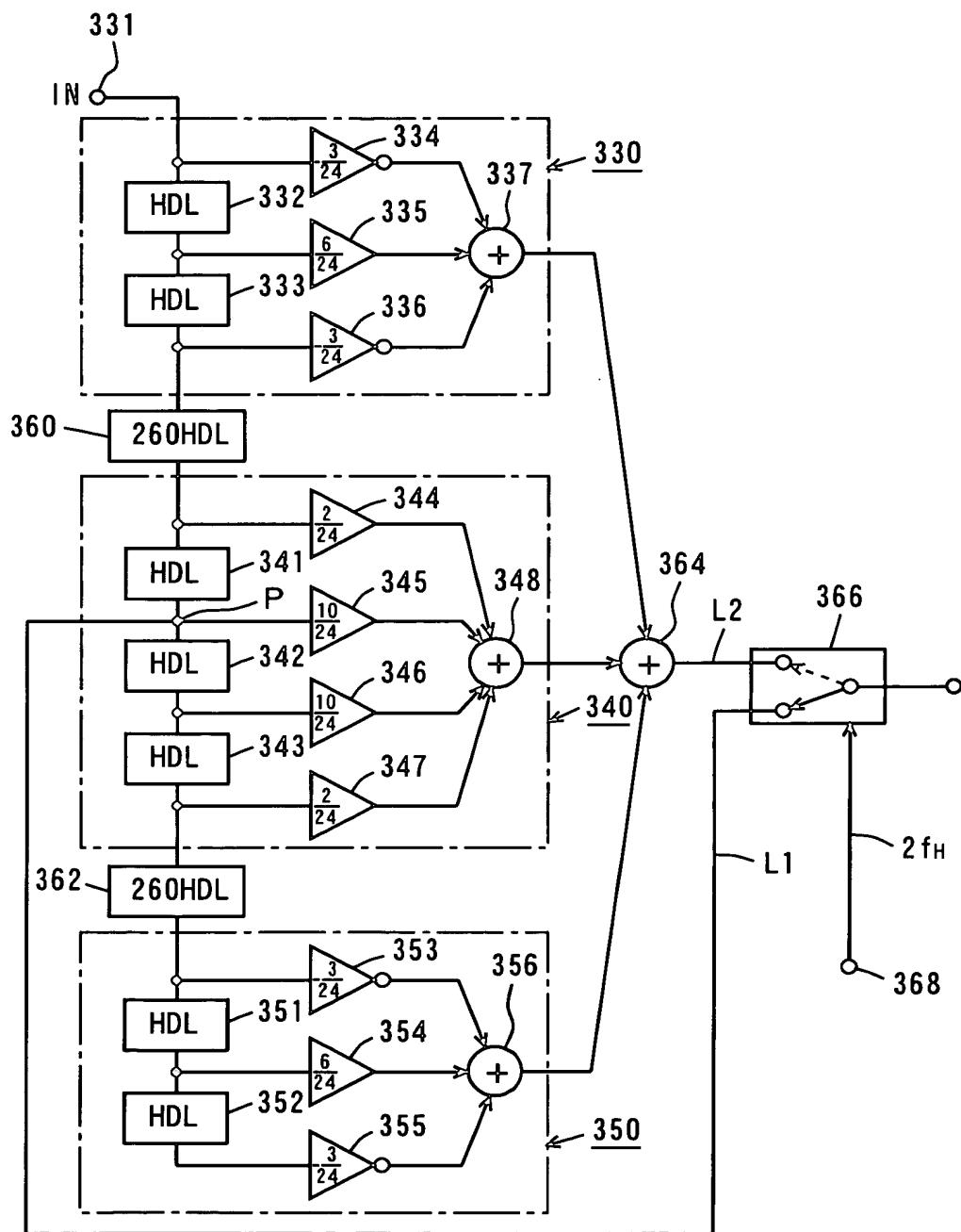
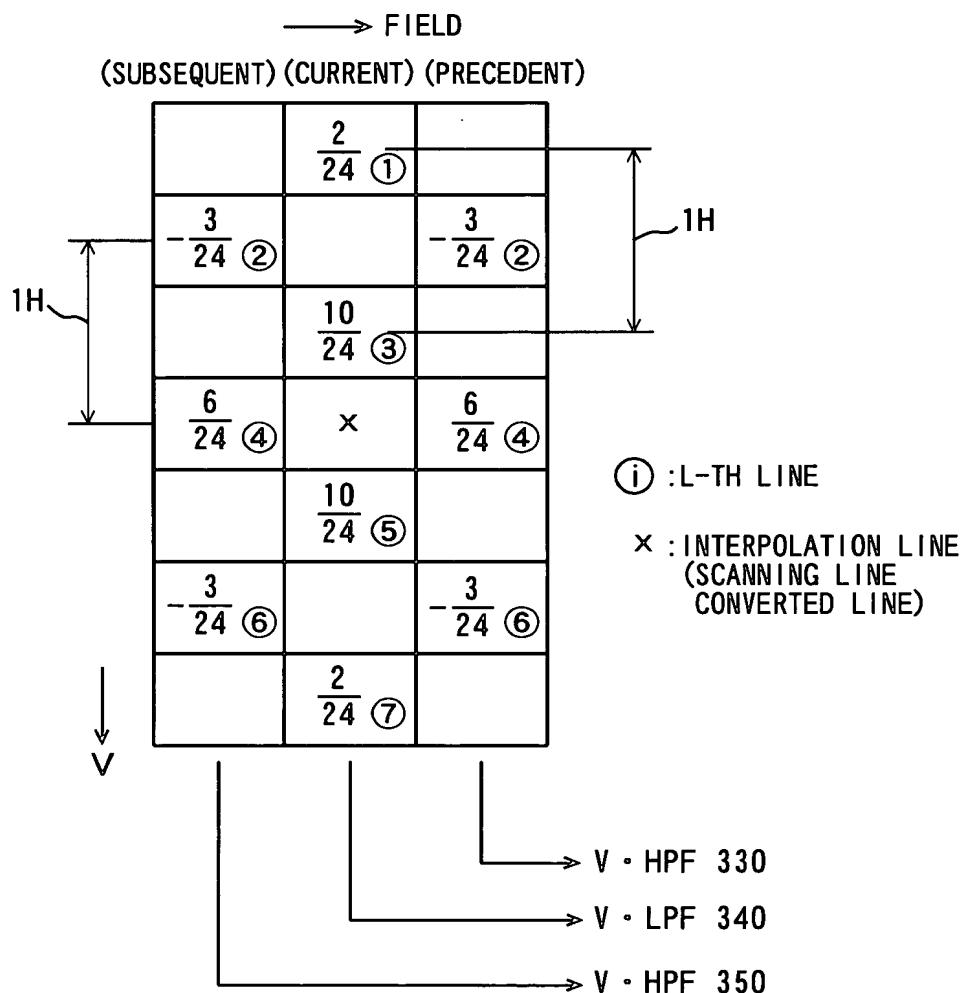


FIG. 36



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FIG. 37

